HIGH DENSITY SEMICONDUCTOR MEMORY CELL AND MEMORY ARRAY USING A SINGLE TRANSISTOR HAVING A BURIED N+ CONNECTION

ABSTRACT OF THE DISCLOSURE

A programmable memory cell comprised of a transistor located at the crosspoint of a column bitline and a row wordline is disclosed. The transistor has its gate formed from the column bitline and its source connected to the row wordline. The memory cell is programmed by applying a voltage potential between the column bitline and the row wordline to produce a programmed n+ region in the substrate underlying the gate of the transistor. Further, the row wordline is formed from a buried N+ layer allowing for higher density integration.